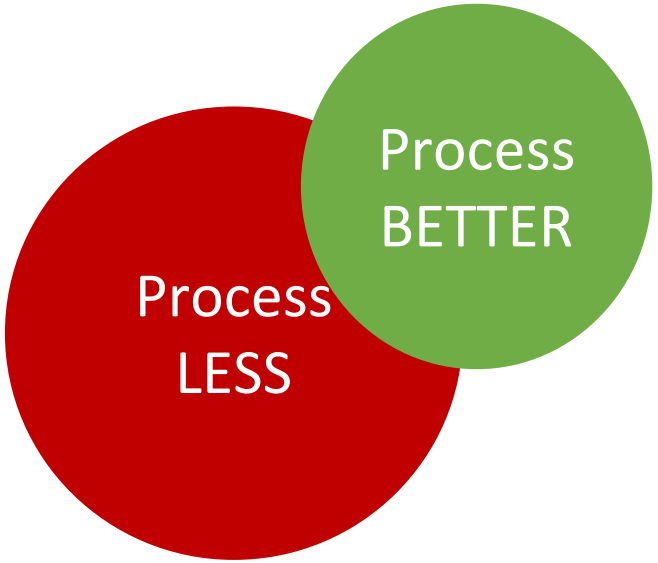
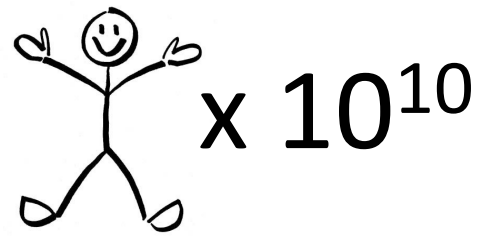
…in 2050





José A. Cobos

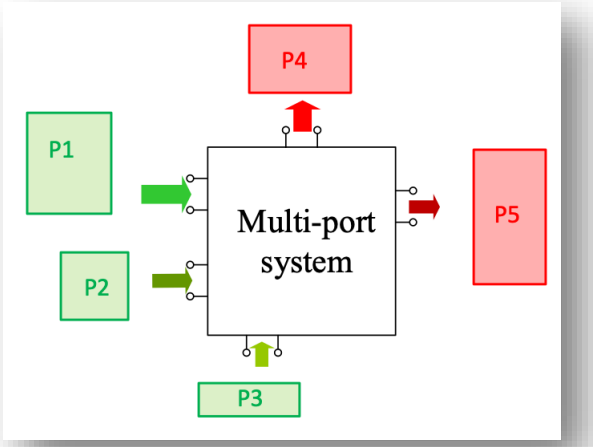
April 1st, 2023

Three Corners Power Electronics Extended Collaboration (3C-PEEC) Workshop

Moving Towards a Carbon-Free World by 2050

#1 Adoption of VA area models

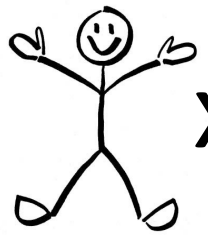
Reconfigure SOURCE, LOAD & power architecture



…in 2050

Process BETTER

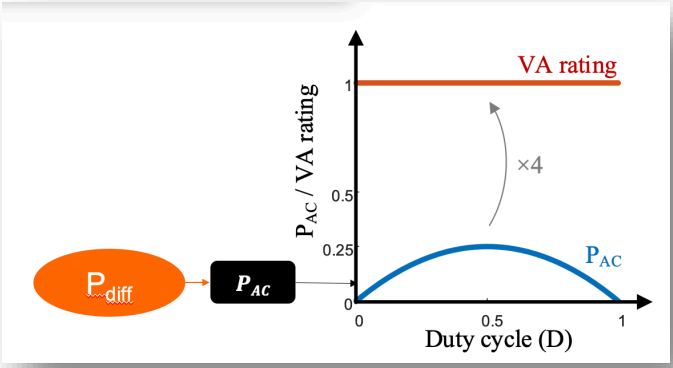
Process LESS



x 10^{10}

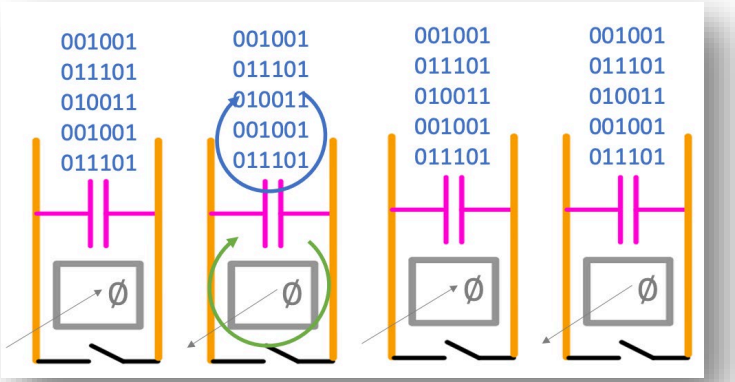
#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss



#3 SURFACE power delivery

Generate LOAD current ubiquotously (Extension of "Point of Load")



José A. Cobos

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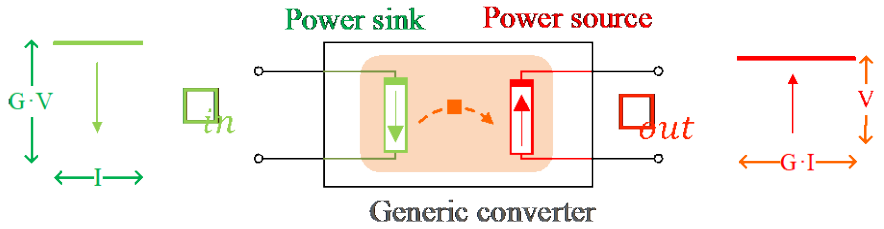
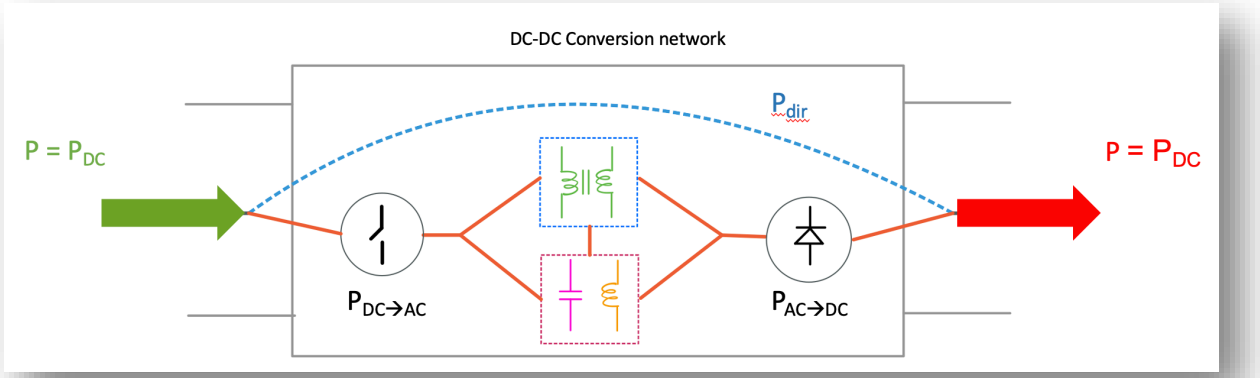
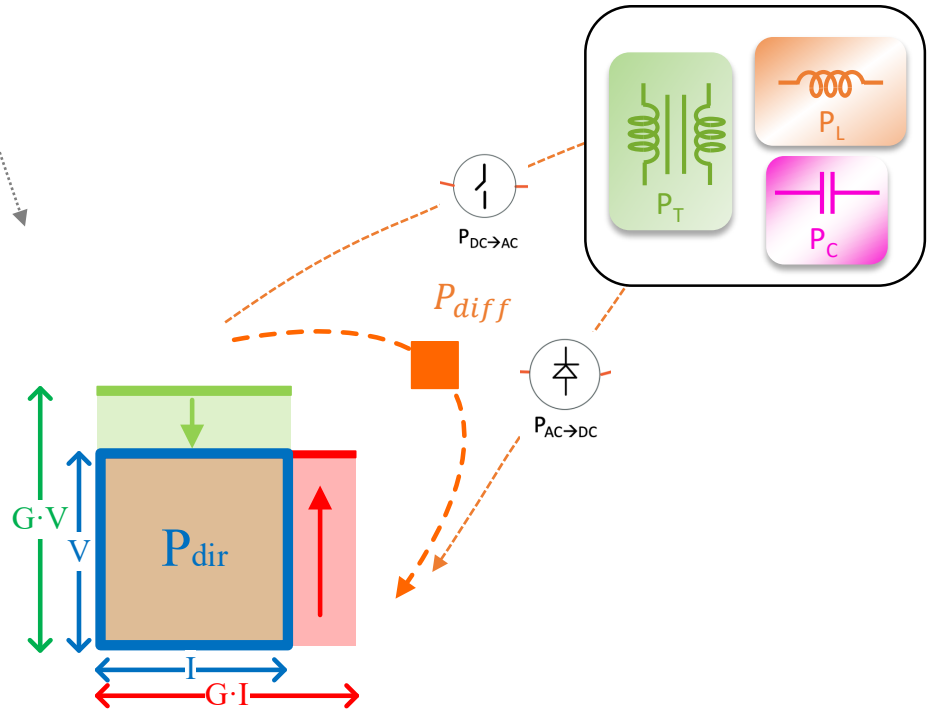
#1 Adoption of VA area models

Reconfigure SOURCE, LOAD & power architecture







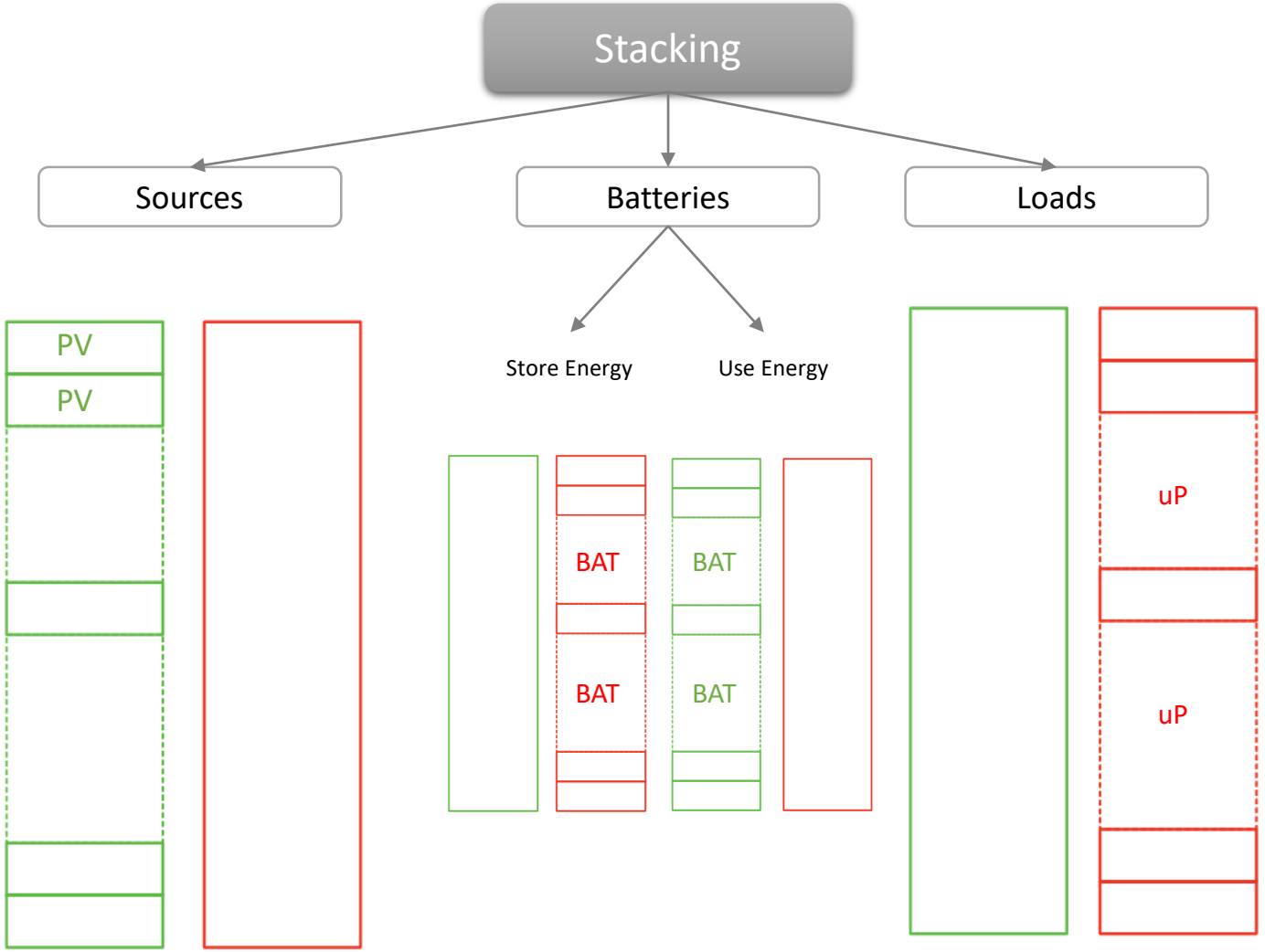
"Processed" Power, instead of **"supplied"** power, is calculated

to SYNTHESIZE Power converters
&
RECONFIGURE sources & Loads

#1 Adoption of VA area models

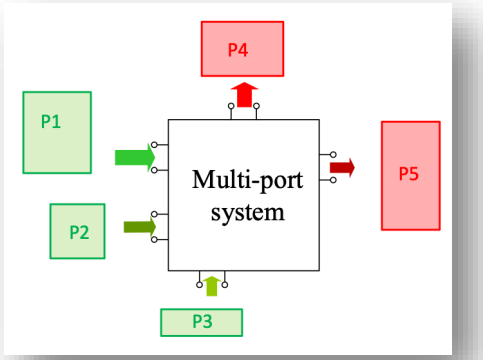
Reconfigure SOURCE, LOAD & power architecture

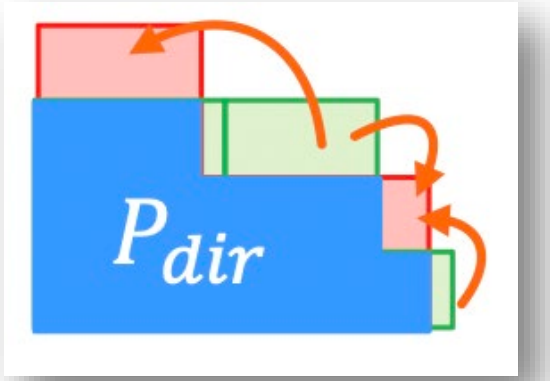
In 2023…



…in 2050

Reconfigurability



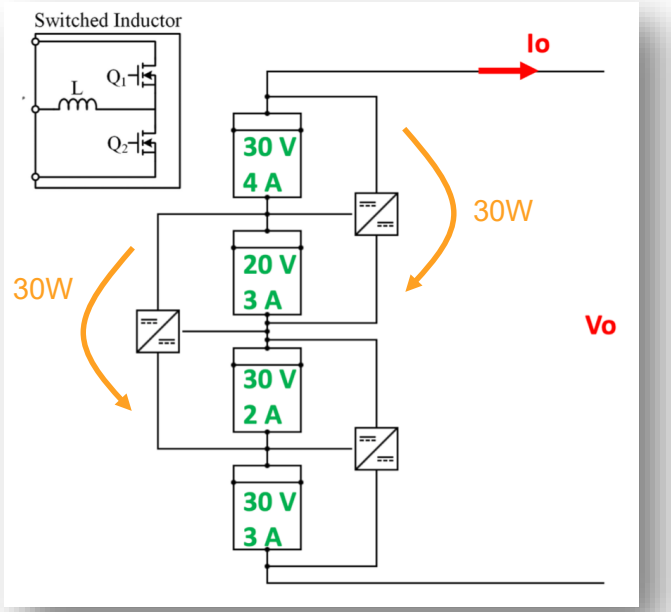


#1 Adoption of VA area models

Reconfigure SOURCE, LOAD & power architecture

In 2023…

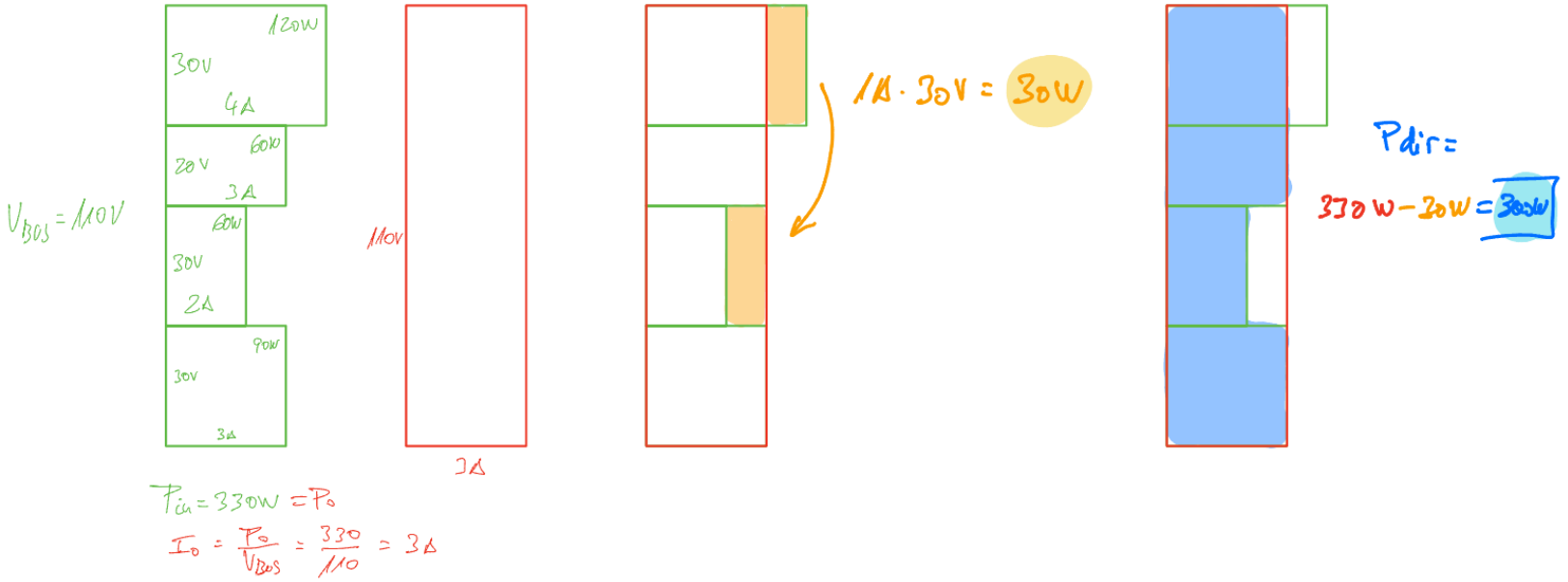
Stacking (DPP)



60W “processed”

330W “supplied”

What is the minimal power to be processed?



30W “processed” !!

…in 2050

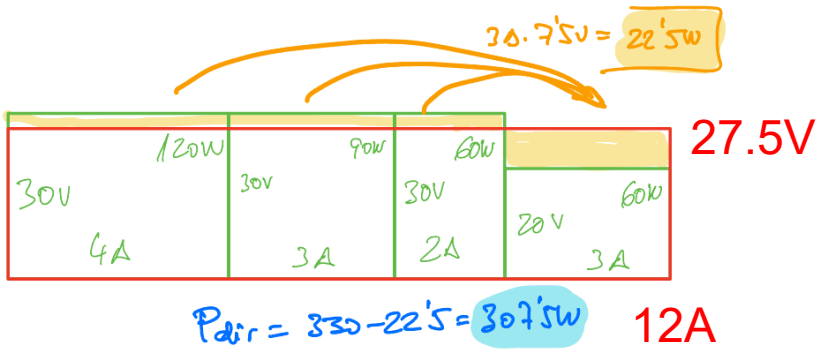
Student quiz at UPM

#1 Adoption of VA area models

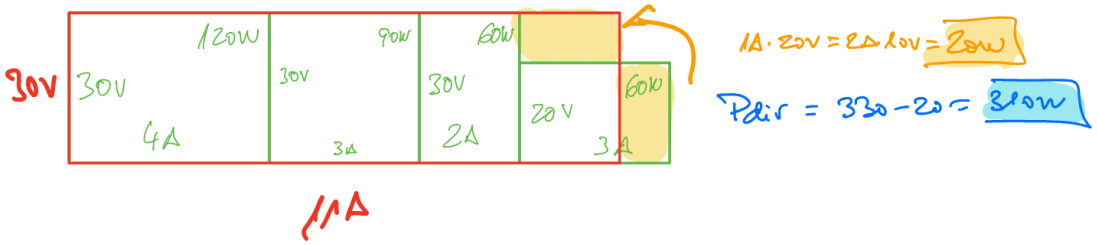
Reconfigure SOURCE, LOAD & power architecture

Reconfigurability

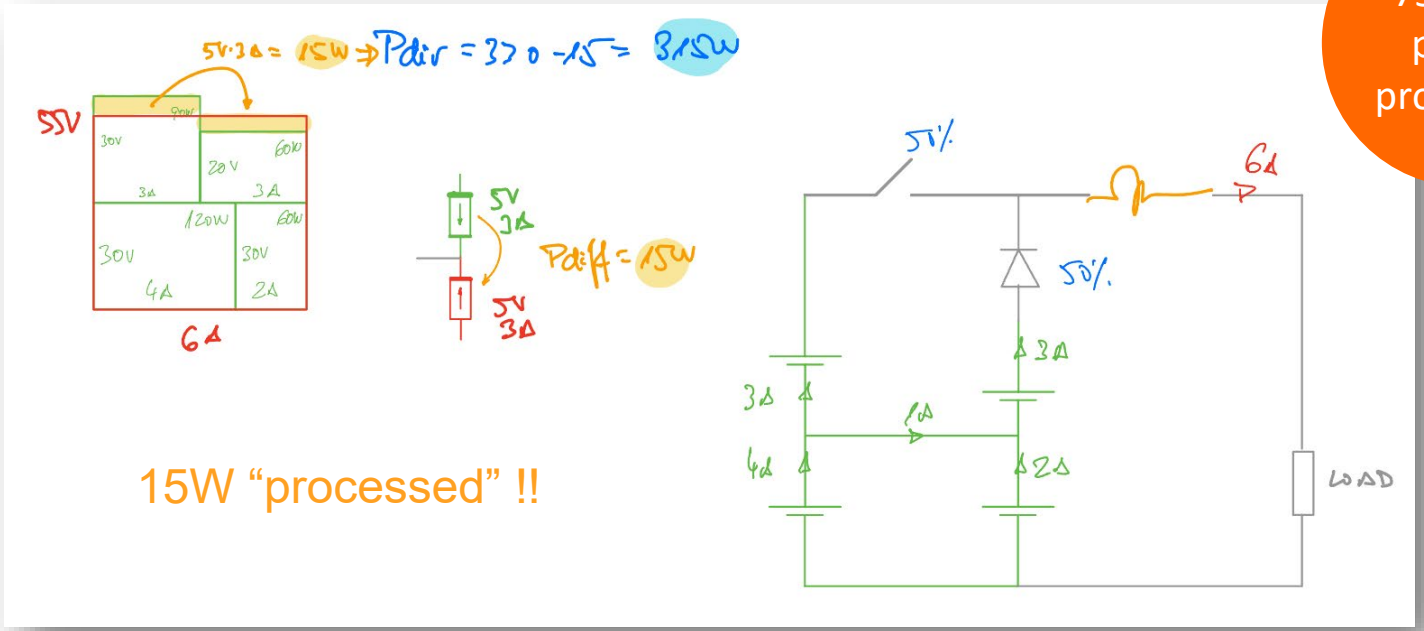
22.5W “processed” !!



20W “processed” !!



75% less power processing



15W “processed” !!

#1 Adoption of VA area models

Reconfigure SOURCE, LOAD & power architecture

In 2023…

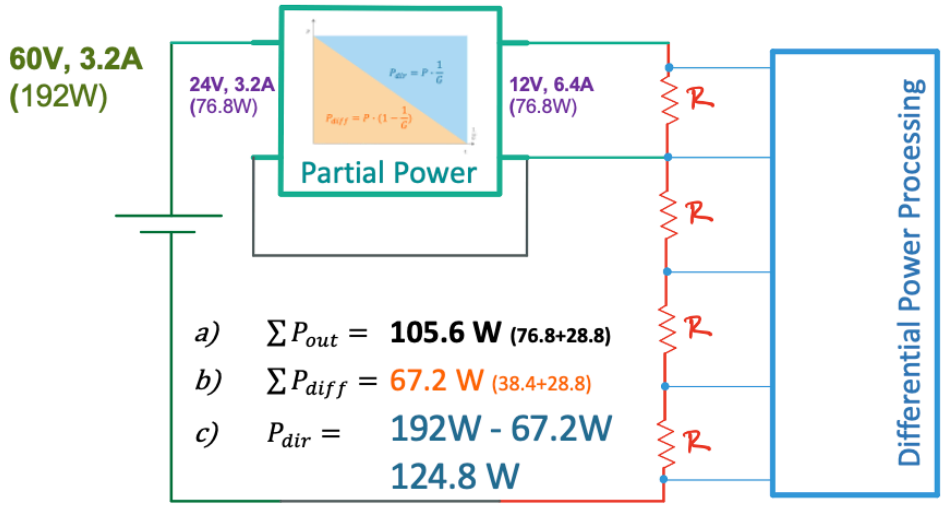
"**supplied**" power is used for optimization

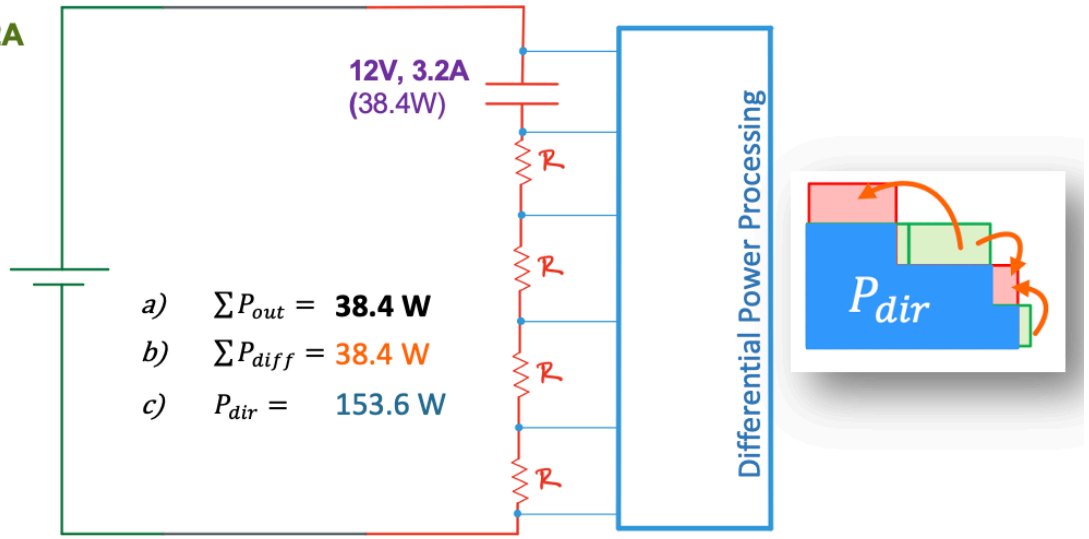
40% less power processing

…in 2050

"**processed**" power is used for optimization

DPP+ Partial Power 67.2W | 38.4W DPP





#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss

Data Centers

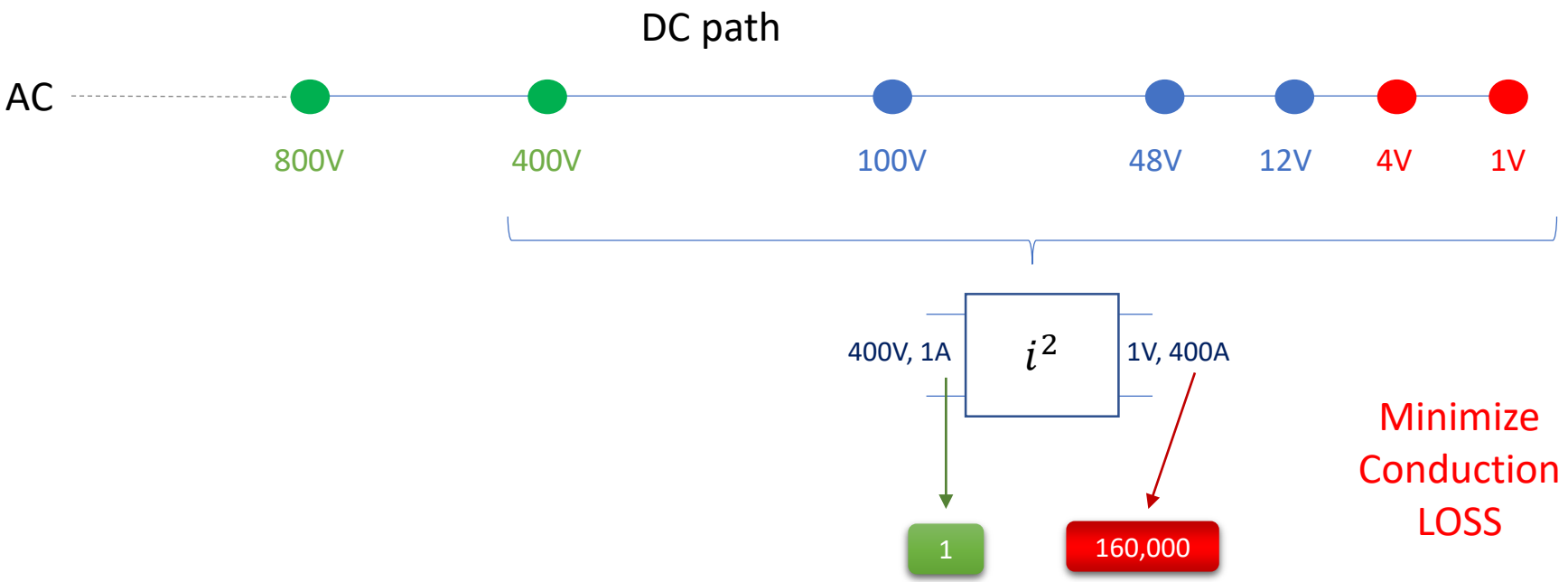
100A → 2000A

(µP) (AI, HPC)

H_2

100's kA

(Electrolysis)



Minimize Conduction LOSS

What is the optimum power topology & power devices for high current applications?

#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss

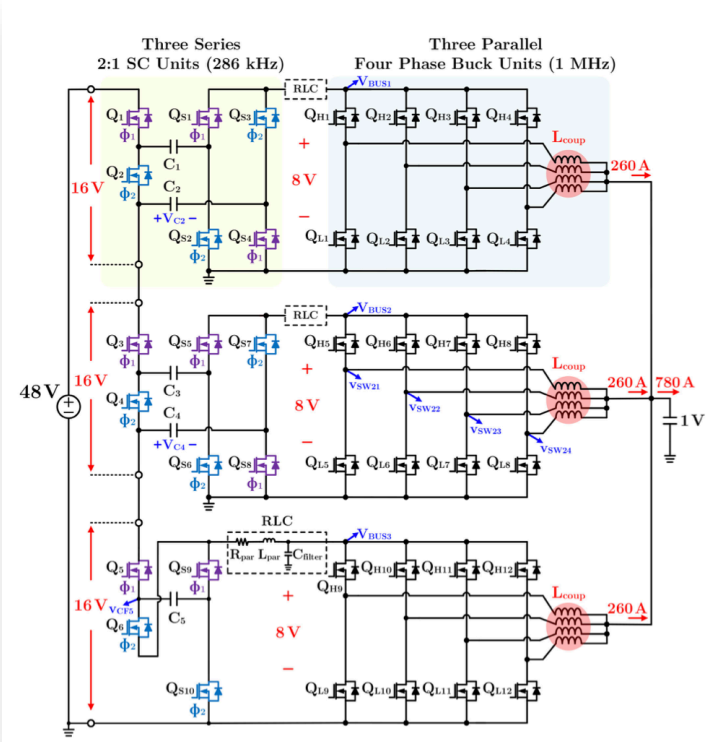
In 2023…

- **50% duty cycle**

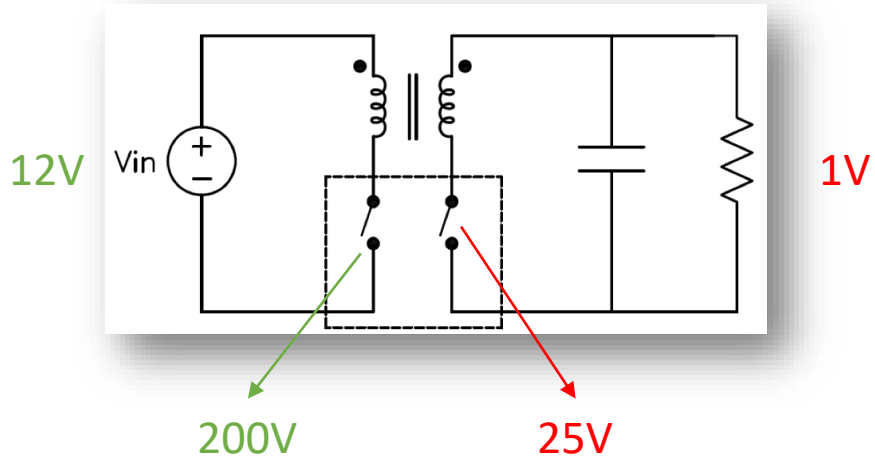
…in 2050

- **90% duty cycle**

"Low Voltage" power switches
for **High Voltage** applications



"High Voltage" power switches
for **Low Voltage** applications



IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 37, NO. 6, JUNE 2022 6305

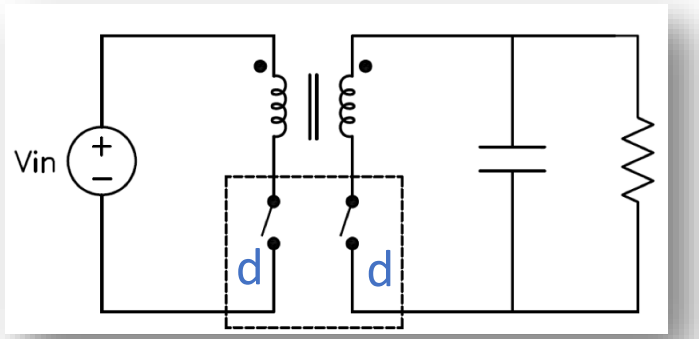
Vertical Stacked LEGO-PoL CPU Voltage Regulator

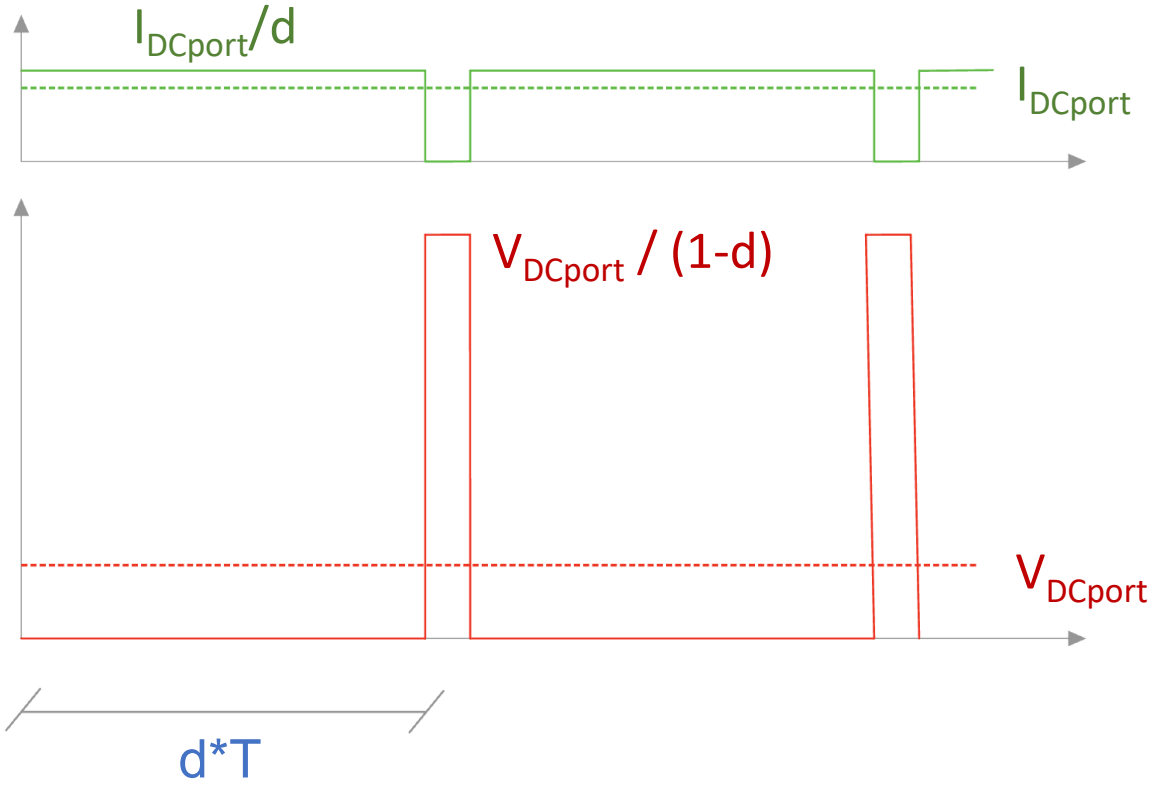
Jaeil Baek, *Member, IEEE*, Youssef Elasser, *Student Member, IEEE*, Kaladhar Radhakrishnan, *Senior Member, IEEE*, Houle Gan, *Senior Member, IEEE*, Jonathan P. Douglas, Harish K. Krishnamurthy, *Senior Member, IEEE*, Xin Li, *Member, IEEE*, Shuai Jiang, *Member, IEEE*, Charles R. Sullivan, *Fellow, IEEE*, and Minjie Chen, *Senior Member, IEEE*

#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss

Optimize for CONDUCTION LOSSES





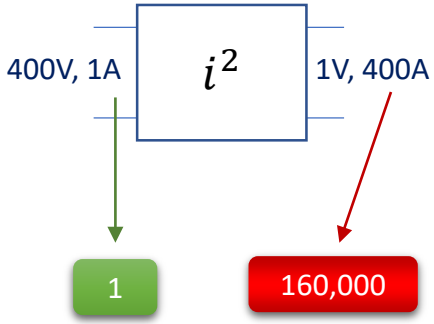
$$i_{rms} = \frac{I_{DCport}}{\sqrt{d}} \longrightarrow Loss_{\boxplus} = \frac{I_{DCport}^2}{d} \cdot R_{DSon\boxplus}$$

Breakdown Voltage

d

#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss



Conduction Loss

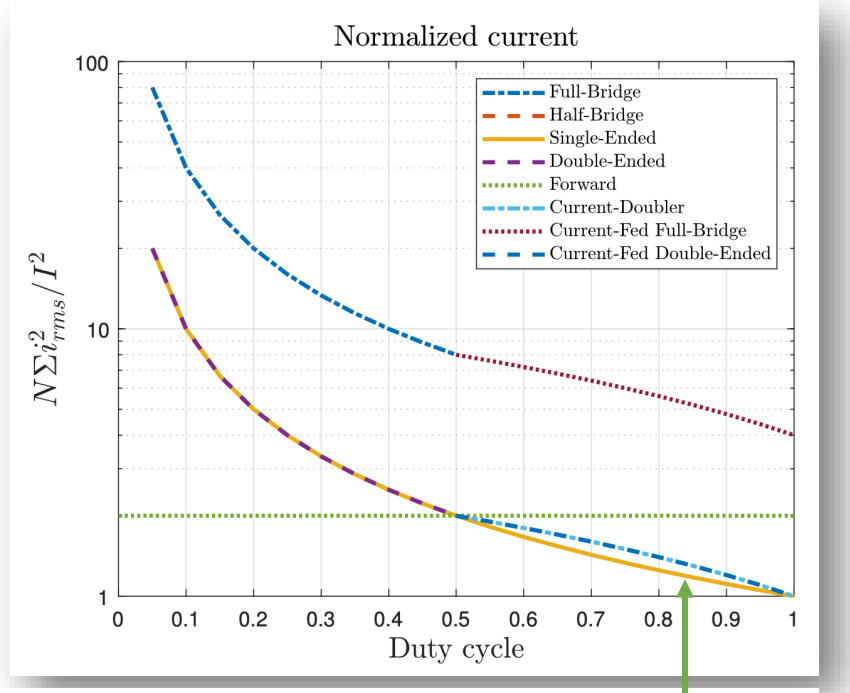
$$Loss_{\boxplus} = \frac{I_{DCport}^2}{d} \cdot R_{DSon\boxplus}$$

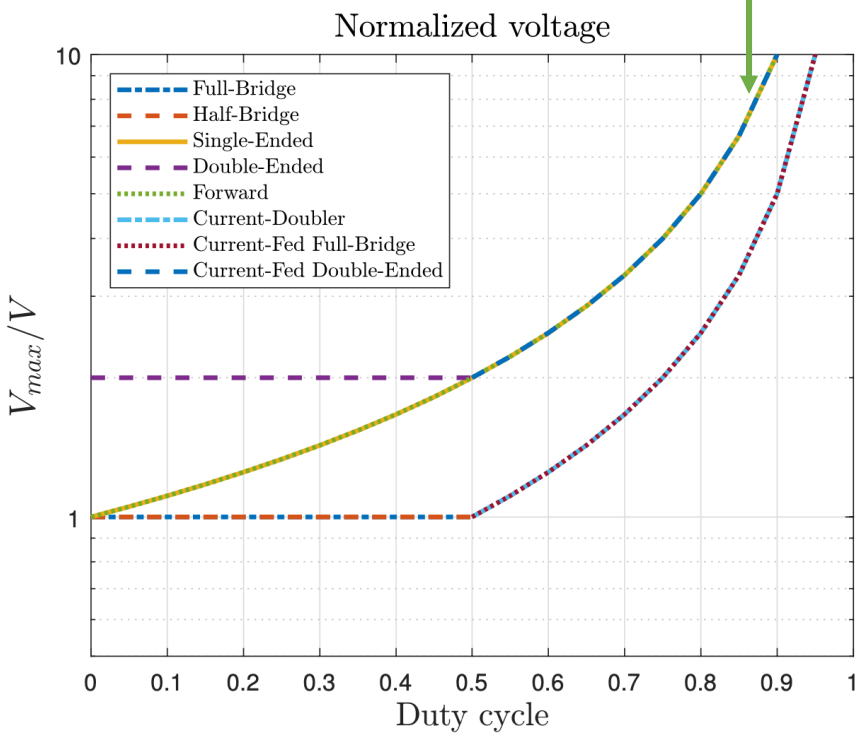
Breakdown Voltage

d

High duty cycle needed

optimum "d"depends on Semiconductor **TECHNOLOGY** (Si, GaN, SiC)





#2 Use HV devices in LV applications

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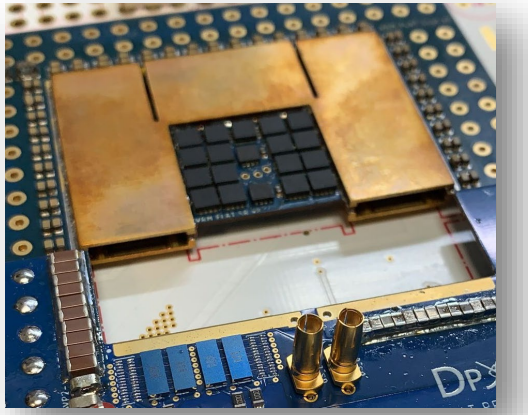
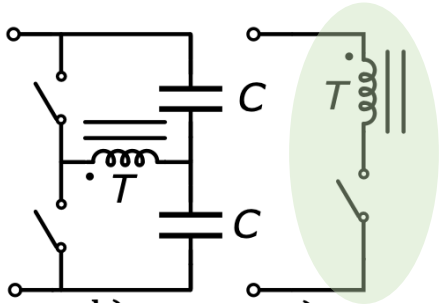


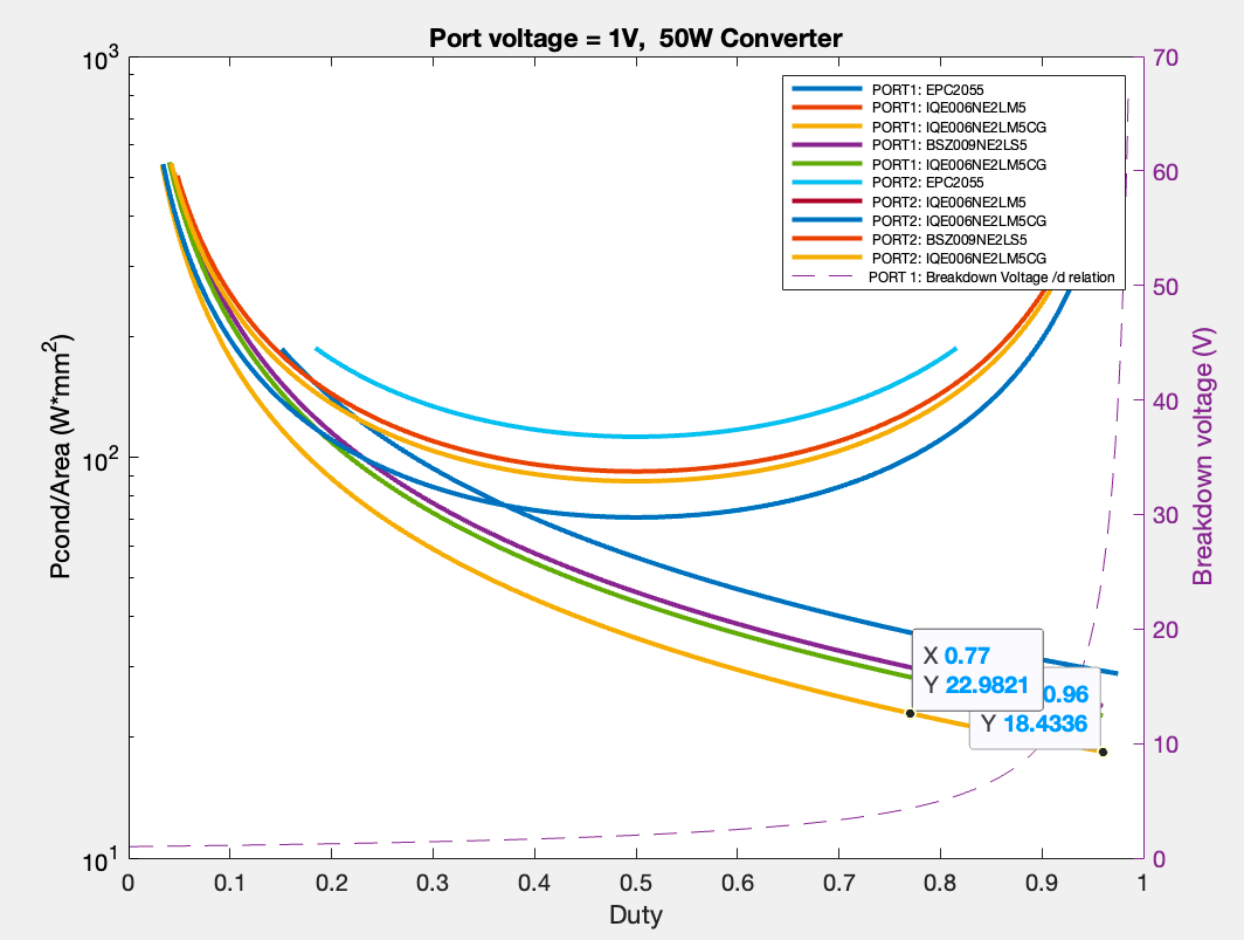


High Voltage - low R_{dson} power switches are needed for high current applications

For 1V output

D=96%

25V devices

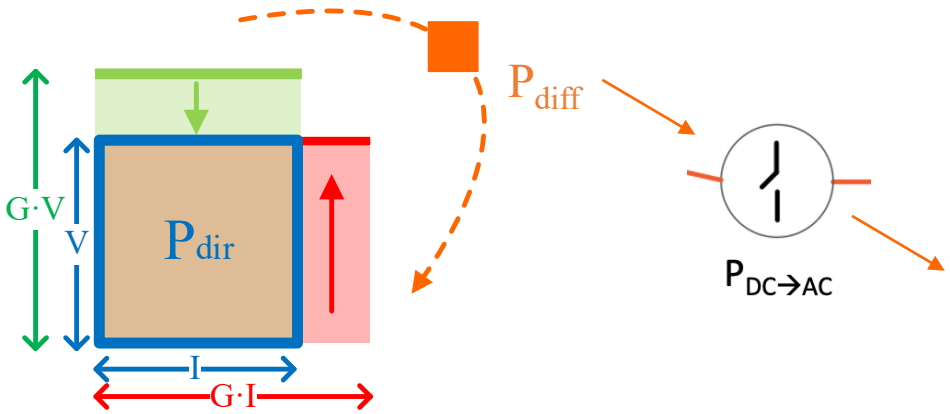


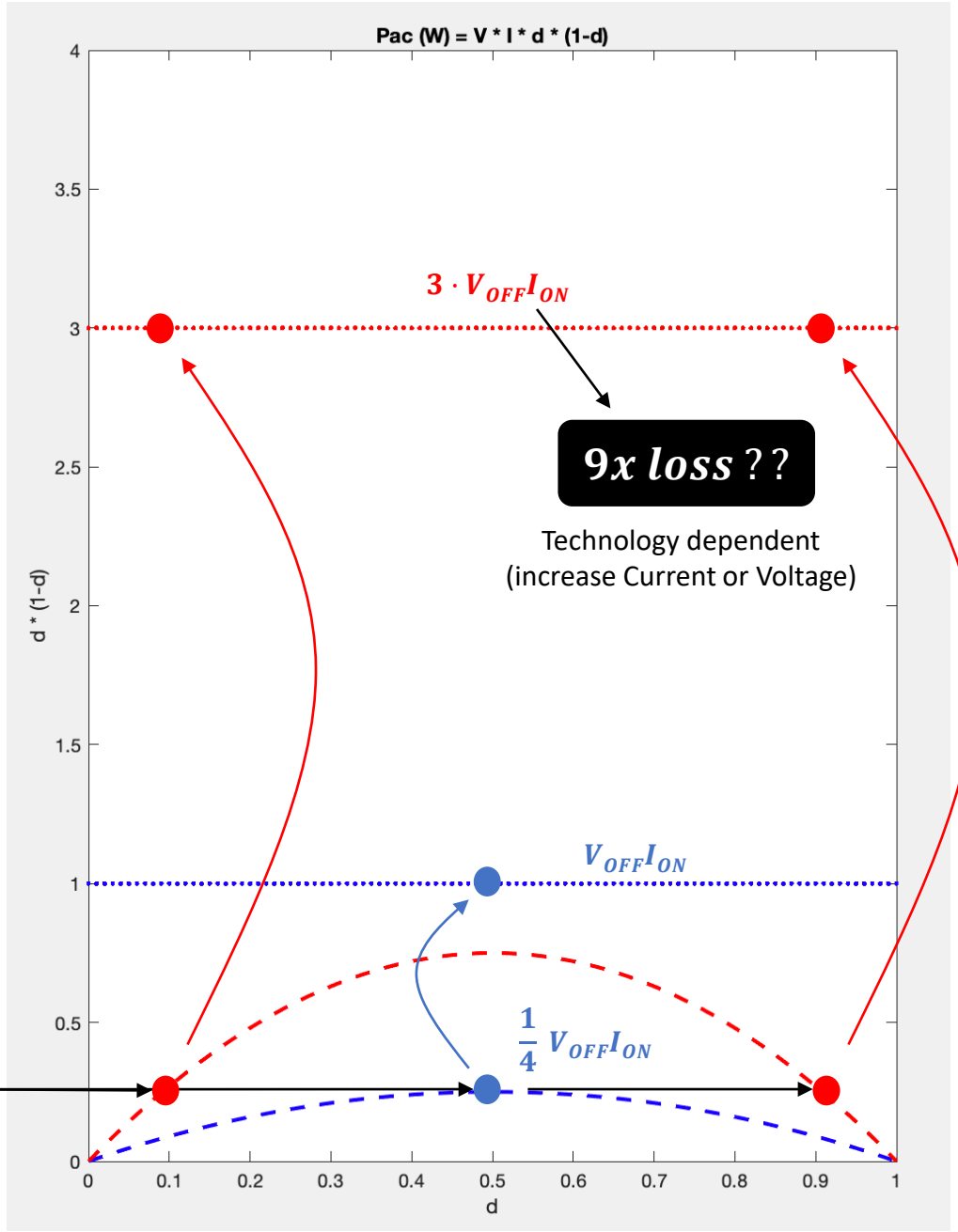
#2 Use HV devices in LV applications

"i" impacts more than "v" on conduction loss

Optimum "D"
50% ??

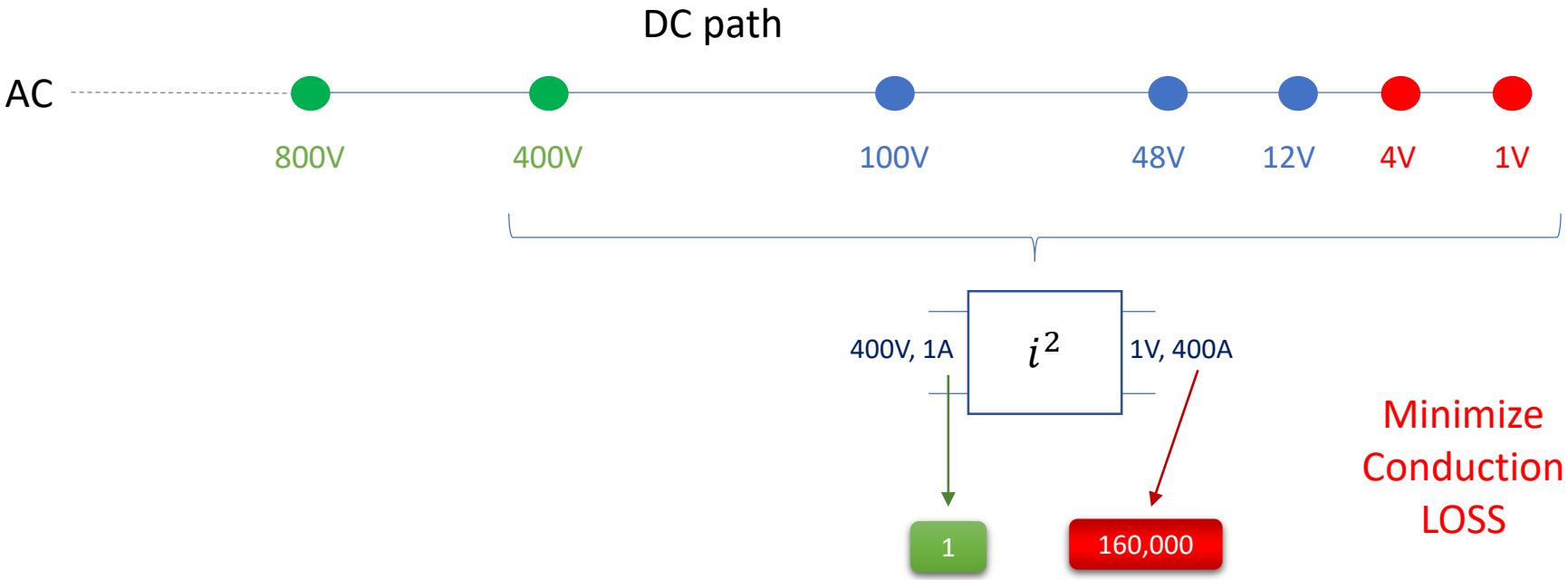
Apparently YES,
but NOT for low voltage, kA applications,
D= 90% is better !!





#3 SURFACE power delivery

Generate LOAD current ubiquotously (Extension of “Point of Load”)



Minimize Conduction LOSS

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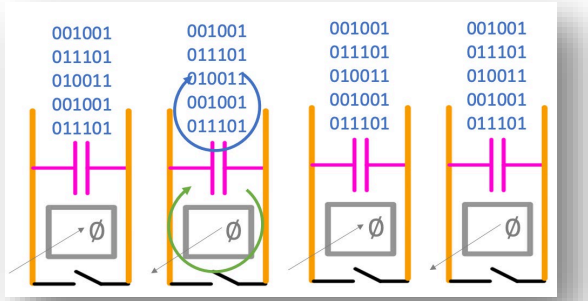
(µP) (AI, HPC)

H_2

100’s kA

(Electrolysis)



What is the optimum delivery path for high current applications?

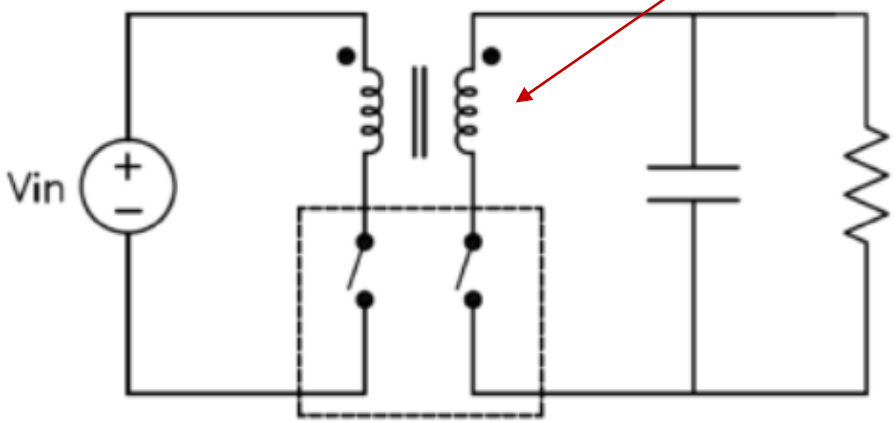
- Generate **load current** “locally”
- Short path

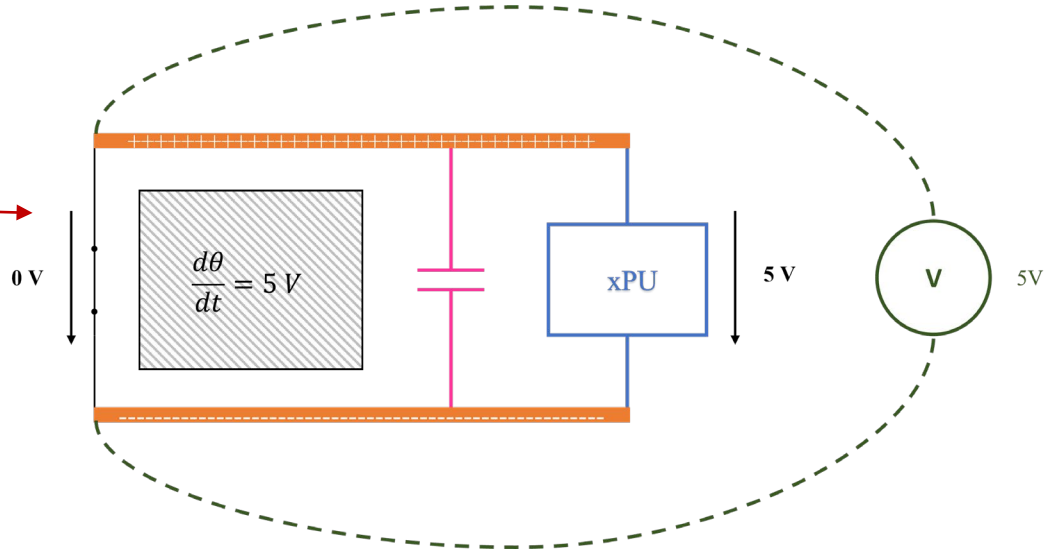
#3 SURFACE power delivery

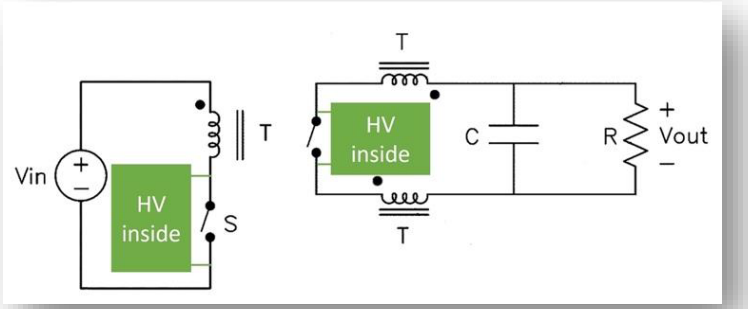
Generate LOAD current ubiquotously (Extension of “Point of Load”)

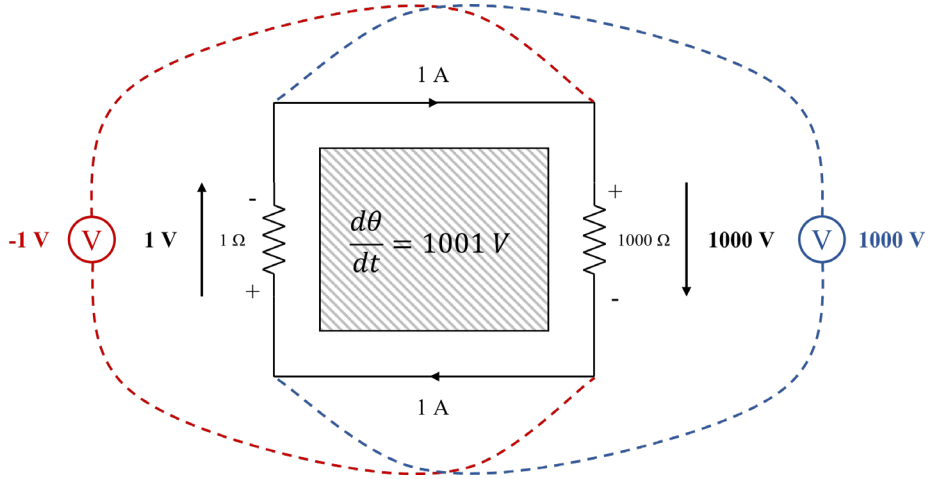
4 segments 1-turn winding

1 turn secondary !



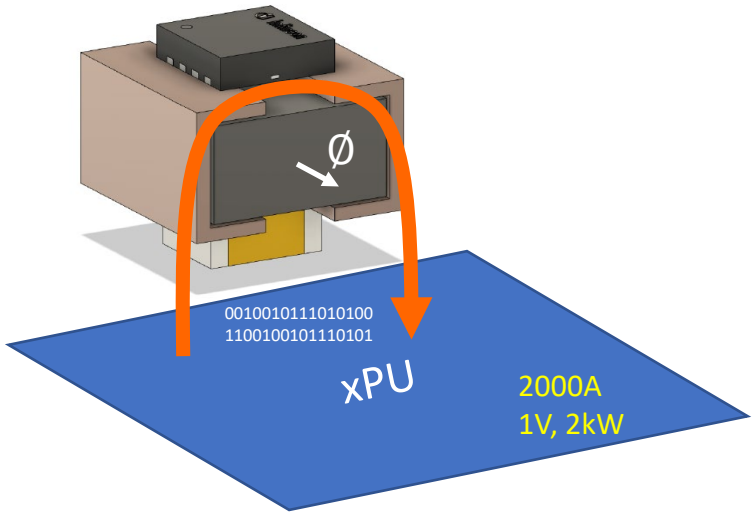




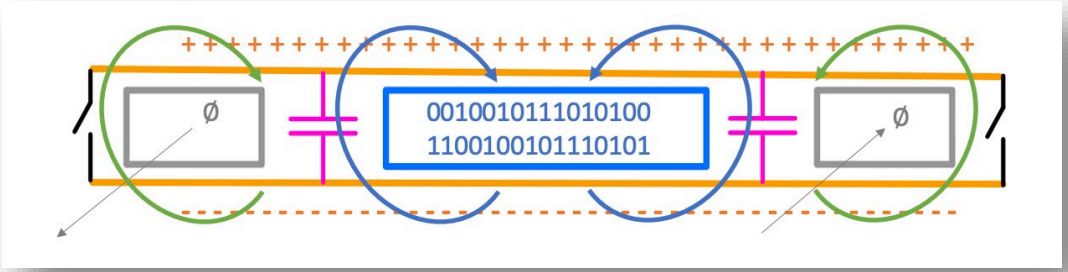


#3 SURFACE power delivery

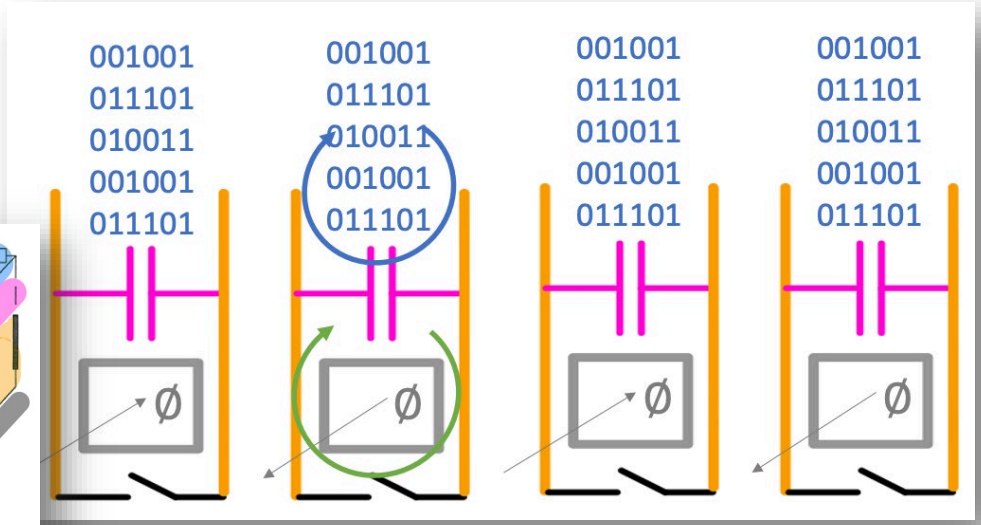
Generate LOAD current ubiquotously (Extension of “Point of Load”)

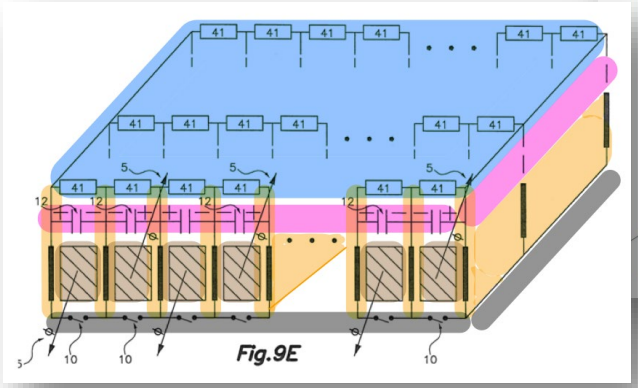


TOP - DOWN



SURFACE



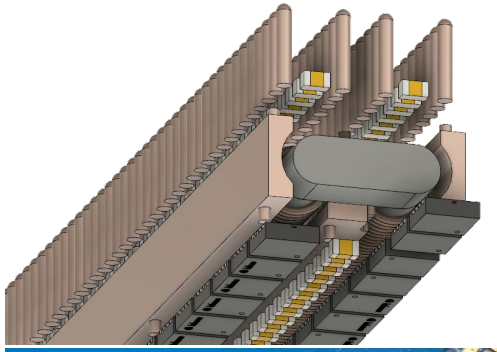


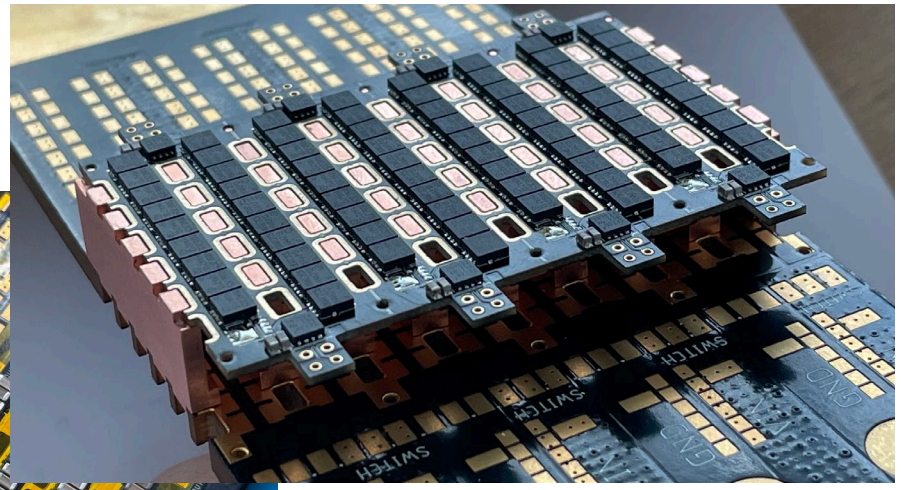
#3 SURFACE power delivery

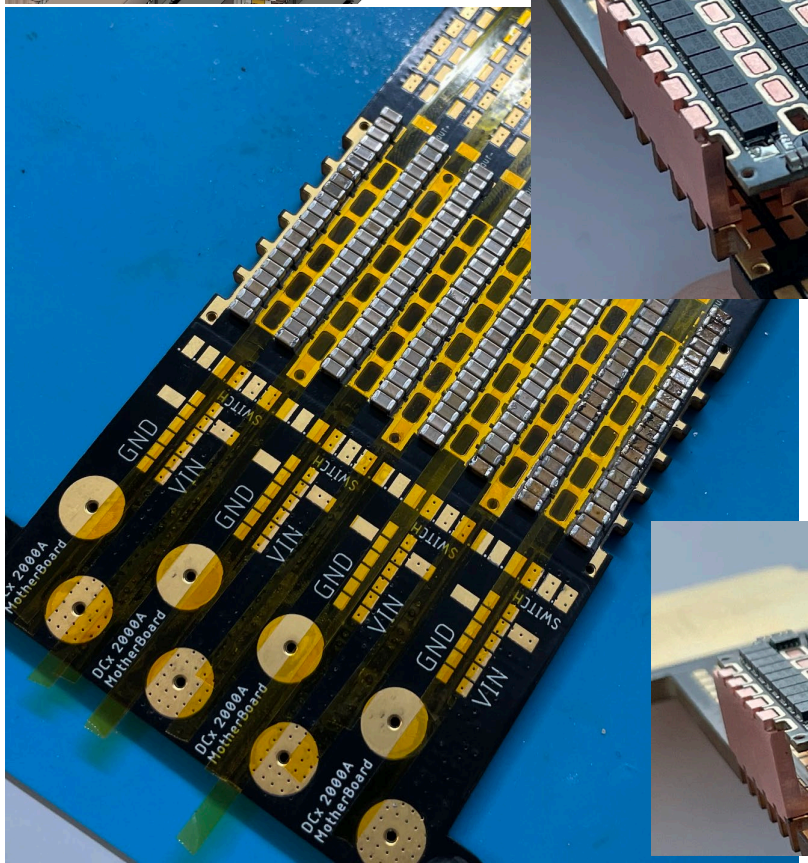
Generate LOAD current ubiquotously (Extension of “Point of Load”)

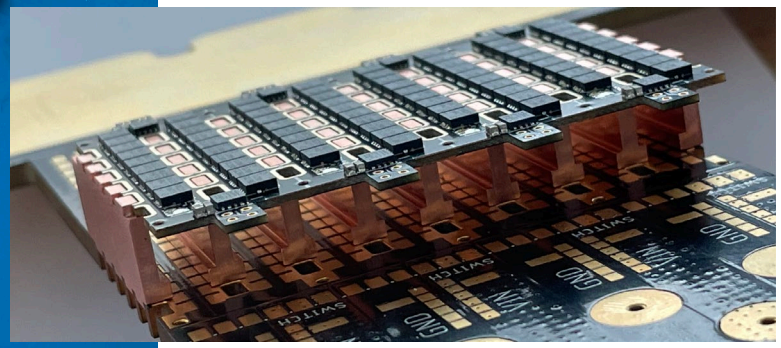
In 2023…

Discrete



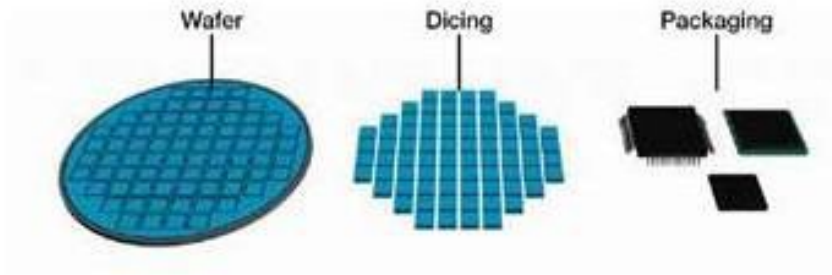






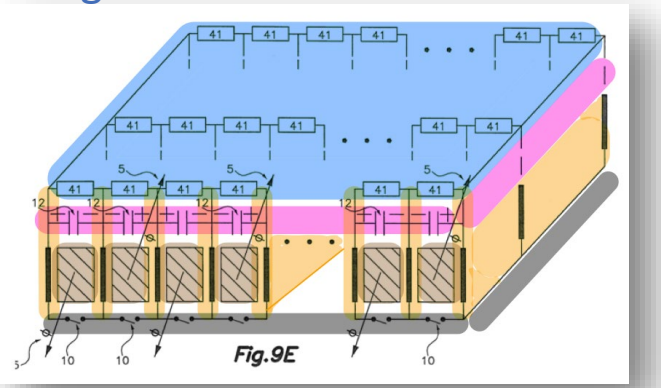
…in 2050

Integrated



http://maltiel-consulting.com/Semiconductor_Manufacturing_101_maltiel-consulting.html

Power conversion is one more layer of the digital circuit



Press headlines

In 2023…	…in 2050

Process Less power

1. RECONFIGURATION of Sources & loads and SYNTHESIS of the power architecture:

• **"supplied"** power is calculated	• **"processed"** power is calculated
• **"stacking"** sources or loads	• **"reconfiguration"** sources & loads
	• **"synthesis"** of power converters

High current (kA) applications requires lower CONDUCTION LOSS

2. HV voltage semiconductors, to reduce RMS current by high duty cycles

• **50% duty cycle**	• **90% duty cycle**
• **FOM: Rxq**	• **FOM: Rxarea**

3. Power Delivery: generate load current (kA) ubiquotously

• **"Lateral" & "Vertical"** power delivery	• **"Surface"** power delivery
• **"Rectifiers"** based on semiconductors	• **"Faradays"** paradox gets rid of the rectifiers

VA models